Fracture on Circuit Board Internal Layers Due to Thermal Stress on Soldered Pins

STW Technic, LP
Mobile Controllers and Measurement Technologies

Felipe Figueroa, Pablo Aguirre
Sensor Technik Wiedemann GmbH, Research & Development Department,
Am Bärenwald 6, 87600 Kaufbeuren, Germany

Introduction: The possibility of circuit board failures are often ignored because they could be easily imperceptible to the naked eye. Actual cracks due to thermal stress on internal layers around a soldered pin via are examined in the present work.

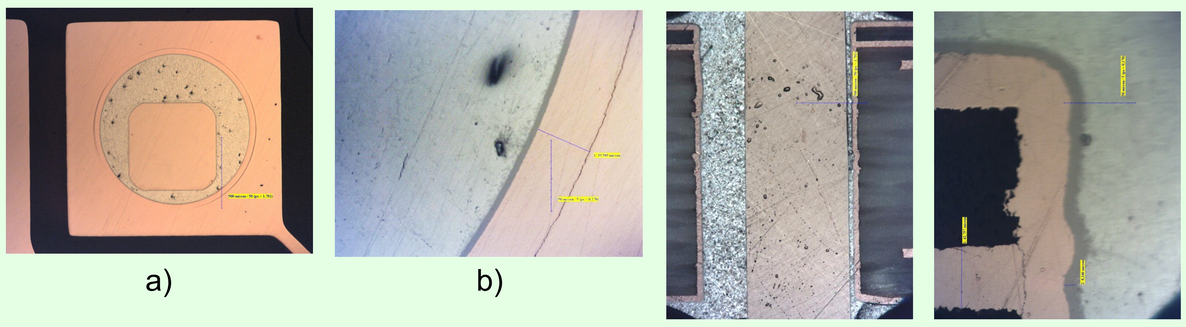

Figure 1. **a)** Upper slice of an inner layer with a soldered pin. **b)** Zoomed region of the fractured layer. **c)** Side cut of the soldered pin and via. **d)** Zoom of the fracture between layer and via.

Temperature changes during the soldering process are modeled, to show the forces involved, determine the breaking points and confirm their plausibility.

Computational Methods: A 2D thermo-mechanical model of a soldered pin is achieved in two simulation steps [1]. First, a soldered pin attached to a fixed circuit board is placed in the via of a secondary circuit board. Being stress and strain free at 21°C, the temperature is raised to 270°C, as in the wave soldering process, which induces the first thermal stresses.

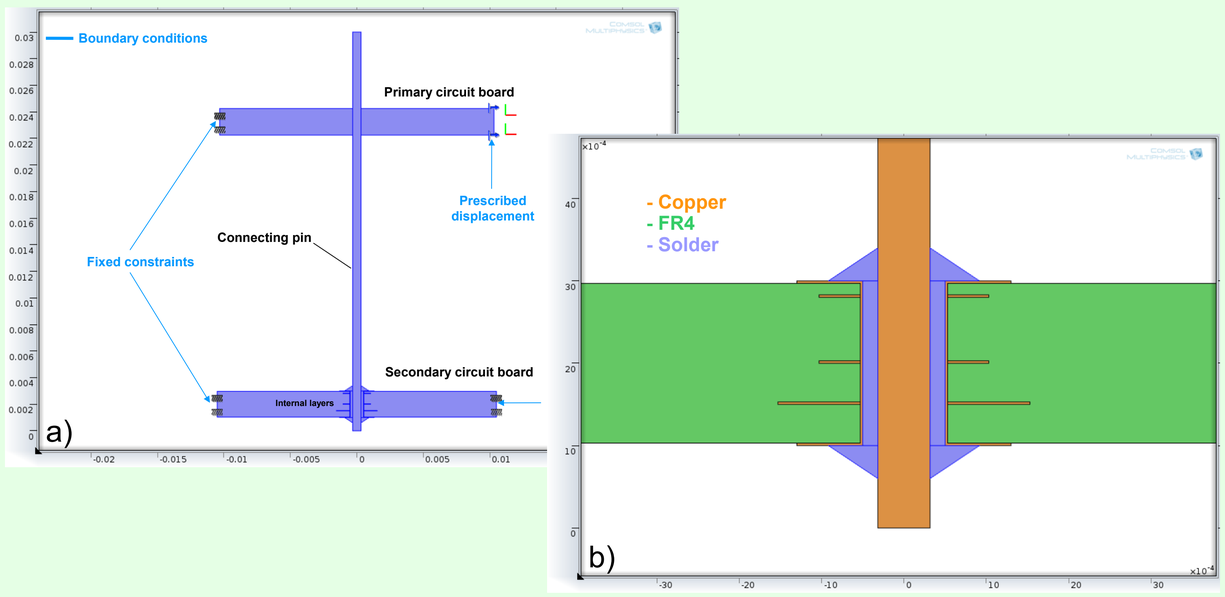

Figure 2. **a)** 2D Model of the simulated construction with boundary conditions. **b)** Close-up of the region of interest and used materials.

Then in the second simulation step, the tin-solder is added in the model between the pin and secondary circuit board. Thermal stresses of the first simulation step are included as an initial stress, and the temperature is finally reduced back to 21°C.

Results: The simulation shows how thermal deformation due to the soldering process, can produce high stresses on the copper layers of the circuit board. Because both circuit boards are fixed, the pin is constantly pulling the soldered area on the bottom board after the system has cooled down.

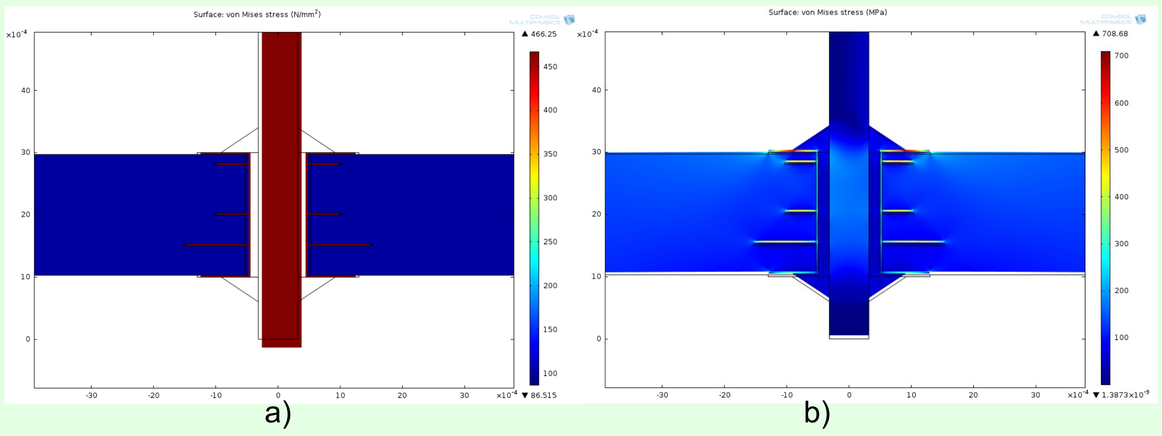

Figure 3. **a)** Heated circuit board and pin before the tin-solder is applied. **b)** Soldered pin after cooling down back to room temperature.

Following a line along the borders of the via, and plotting the stress, clearly shows the magnitudes involved around the weakest areas and the potential generation of fissures.

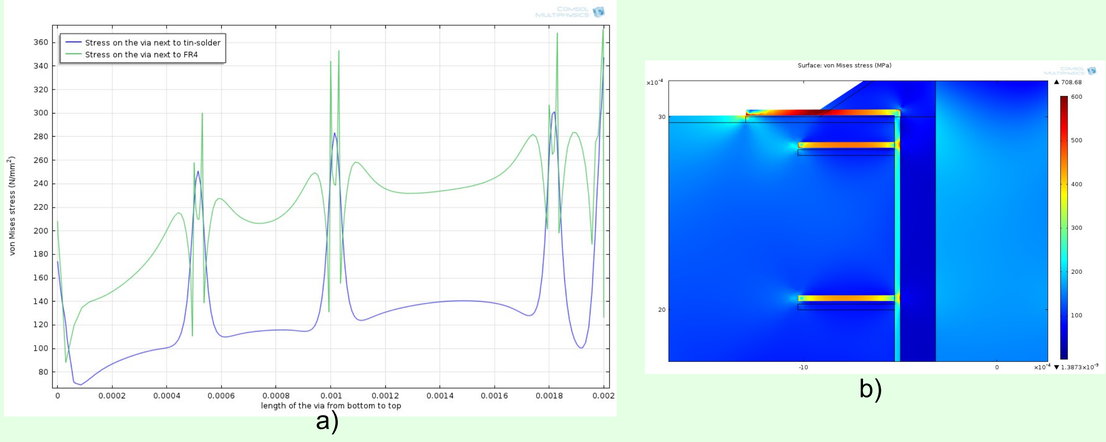

Figure 4. **a)** Stress plot along the borders of the via from bottom to top. **b)** Close-up of the via and layers under stress

Conclusions: Soldered pin connector interfaces used on expansion boards of electronic circuits, could produce high stresses over the board connecting vias when the boards are fixed to other structures before the soldering process takes place. Analyzing the forces involved on the internal layers, demonstrates the possibility of rupture of the traces in connecting areas.
This simple simulation has made possible to better understand a source of failure, optimize the related assembling process to avoid such hazards, and thus improve the quality of the product.

References:

[1] Structural Mechanics Module, Model Library, Thermal-Structure Interaction. COMSOL 4.3b.

Excerpt from the Proceedings of the 2013 COMSOL Conference in Rotterdam