Estimating Parasitic Capacitances in MEMS Microphones using Finite Element Modeling

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Abstract

This paper describes the approach to estimate the parasitic capacitances in the MEMS microphones using Finite Element Modeling technique. The parasitic capacitances are generally the acoustically inactive section that deteriorates the electro acoustics performance of the microphone. Therefore, a good estimation of parasitic capacitance is very important to help in improving the acoustic characteristic of microphone. The Finite Element Modeling with Comsol Multiphysics® simulation software can help in predicting the inactive capacitances directly with better accuracy.

Keywords: MEMS Microphone, Parasitic Capacitance, Finite Element Modeling

Introduction

A MEMS microphone is an electro acoustic transducer that converts an acoustic signal into an electrical signal. MEMS microphone are widely used in applications such as cell phones, hearing aids, audio systems etc. ranging from Automobile, Aerospace, Healthcare and Consumer Electronics. Capacitive microphones are most common due to their low power and tolerance to high temperature. MEMS microphones consists of a conductive back plate and a conductive flexible membrane. The back plate and the membrane are at a certain distance from each other and may be interpreted as parallel plates of a capacitor. When a bias voltage is applied to the electrodes, membrane deflection caused by received acoustic signals are converted into electrical signals which are then processed by the ASIC signal chain. The microphone consists of a central region and an outer perimeter region. The central region is the active region of the microphone which is acoustically active. This central region is surrounded by the outer perimeter region that is acoustically inactive. In the outer perimeter region, there is a formation of inactive capacitance between the membrane and substrate as well as between back plate and substrate.

The accurate prediction of parasitic capacitance is today`s subject of advanced research in many MEMS state-of-the art devices and integrated circuits. The fringing field can generate fringing capacitance and often contribute to the overall capacitance, and this should not be ignored.

Models have been implemented based on the design to estimate these inactive capacitances using the AC/DC Electrostatics module provided by COMSOL Multiphysics® simulation software tool. Electric potential and Electric field distribution is plotted. The FEA results obtained seems to match well with the analytical calculation as well as experimental results.

Theory

Consider a simple rectangular wire placed above the semiconductor substrate, as shown in Figure 1. If the width of the wire is substantially larger than the thickness of the insulating material, it may be assumed that the electrical field lines are orthogonal to the capacitor plates, and that its capacitance can be treated as the parallel-plate capacitor model. Under those circumstances, the total capacitance of the wire may be simply approximated as

$$C = (\varepsilon_{di}/t_{di}) * WL \quad (1)$$

where, W and L are respectively the width and length of the wire, t_{di} and ε_{di} represent the thickness of the dielectric layer and its permittivity.

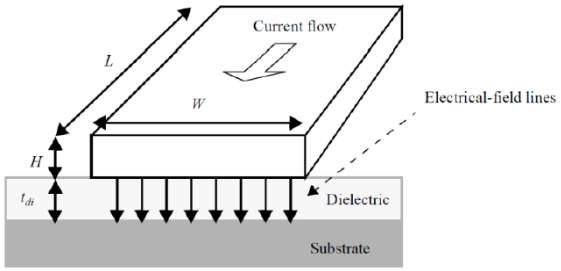


Fig.1 Parallel-plate capacitance model of trace wire.

The capacitance between the side-walls of the wires and the substrate, called the fringing capacitance, also contribute to the overall capacitance, and should also be considered.

The approximate capacitance represented as the sum of two components is as shown in Figure 2: a parallel-plate capacitance determined by the orthogonal field between a wire of width *W* and the ground plane, in parallel with the fringing capacitance modeled by a cylindrical wire with a dimension equal to the interconnect thickness H [1]. The resulting unit capacitance (*pF/μm*) can be written as

$$C_{wire} = C_{pp} + C_{fringe} = W.\ \varepsilon_{di}/t_{di} + (2\pi\varepsilon_{di}/\log(t_{di}/H))$$

With $w = W - H/2$ a good approximation for the width of the parallel-plate capacitor. Numerous more accurate models [2] have been developed over time, but these tend to be substantially more complex, and defeat our goal of developing a conceptual understanding.

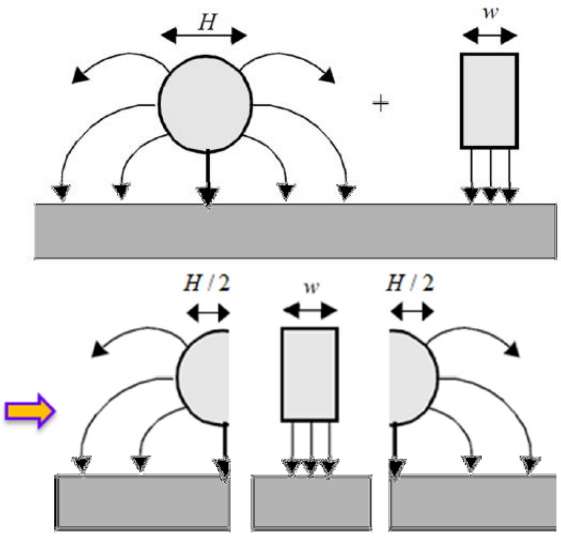


Fig.2 The fringing-field capacitance.

The model decomposes the capacitance into two contributions: a parallel-plate capacitance, and a fringing capacitance, modeled by a cylindrical wire with a diameter equal to the thickness of the wire [1]. The cross sectional view of a typical MEMS microphone device is as shown in Figure 3.

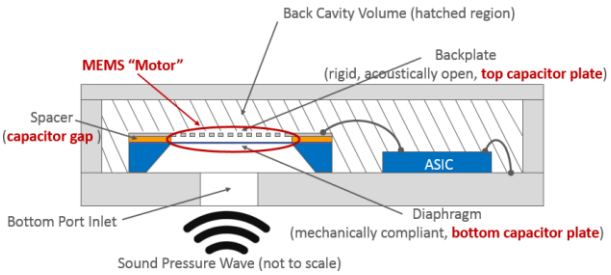


Fig.3 Cross-section representation of a capacitive microphone

Figure 4 represents the active and inactive capacitances formed in a typical microphone device as discussed in the previous section.

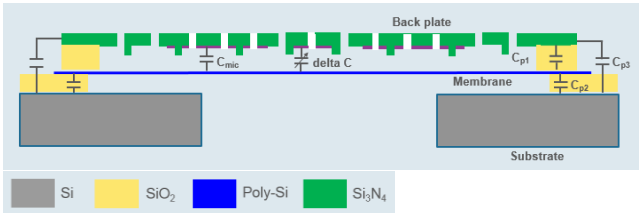


Fig.4 Formation of active and inactive capacitances

As marked in the above figure, the C_{mic} is the active capacitance and delta C is due to change in the gap between diaphragm and back plate due to acoustic pressure applied. The inactive capacitances include Cp_1, Cp_2 and Cp_3 formed between diaphragm, back plate and substrate.

The equivalent circuit for parasitic capacitance formation is represented in a simplified way as shown in figure 5.

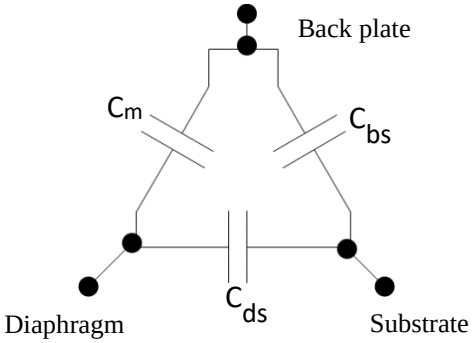


Fig.5. Equivalent circuit

Cds consists of two components. Cds-Bond pad, which is parasitic capacitance between diaphragm and bond pad and Cds-Diaphragm-Substrate overlap which is parasitic due to diaphragm and substrate overlap. In normal operation, the membrane and bulk are shorted together and biased at ground to eliminate Cp_2.

The top view of the microphone is shown in figure 6. The substrate/diaphragm bond pads and back plate metal/bond pad are indicated as (a) and (b) respectively.

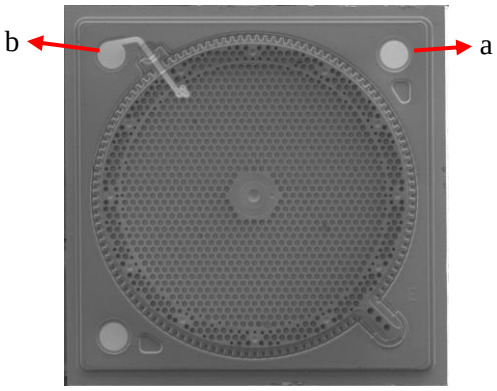


Fig.6. Top view (SEM image) of a designed microphone

Simulation Setup

2D and 3D models have been implemented to estimate the parasitic capacitance in the AC/DC module of the COMSOL Multiphysics® simulation software. Electrostatics physics setup is used to calculate the capacitance between the diaphragm and substrate and back plate and substrate. Electric potential and electric field distribution can be easily plotted with the help of COMSOL Multiphysics® simulation software.

The cross section of bond pad is as shown in figure 7. Moving from bottom to top order there is Substrate, PSG/oxide material, Poly Silicon and Metal.

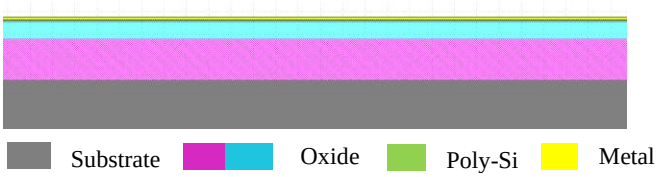
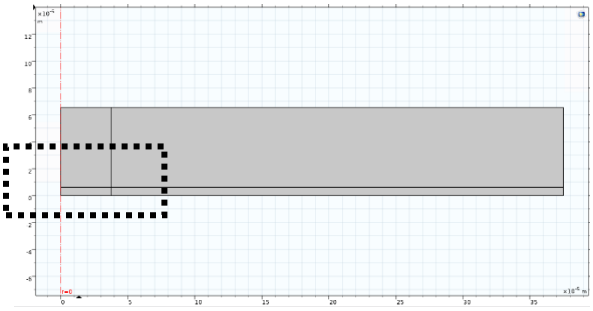


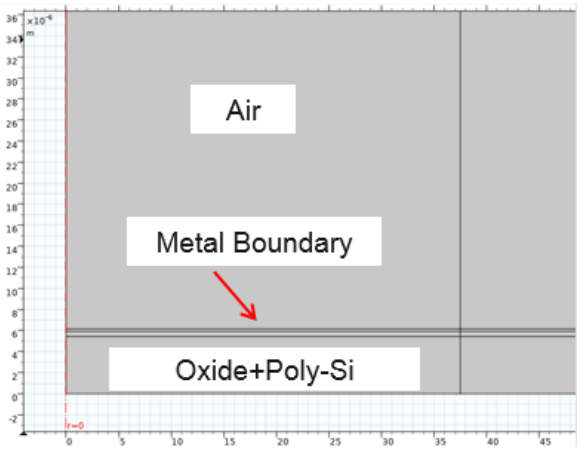
Figure 7. Cross section of Bond pad

A 2D axisymmetric model is set up for calculating the parasitic between bond pad and diaphragm as shown in figure 8. The dimensions used in this model are tabulated in table 1.

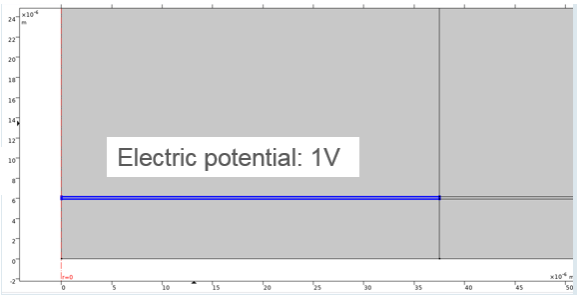
Table 1

Parameters	Value
Bond pad radius	37.5 um
PSG/Oxide layer thickness	5.425 um
Metal thickness	0.25 um
Polysilicon thickness	0.5 um





The zoomed in image of the section highlighted is shown above. The physics set up is done under AC/DC module for Electrostatics and stationary study. The boundary conditions includes applying an electric potential of 1V on the metal boundary and grounding the substrate as shown in figure 9.



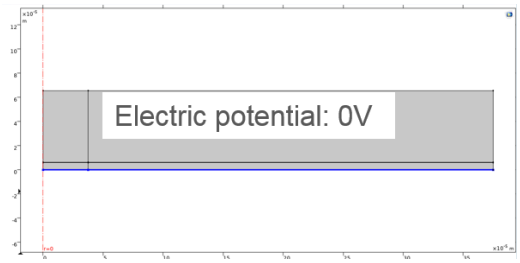


Fig. 9. Boundary conditions applied on the Metal layer and the Substrate

The electric field distribution and electric potential are plotted as shown in figure 10 with zoomed in view.

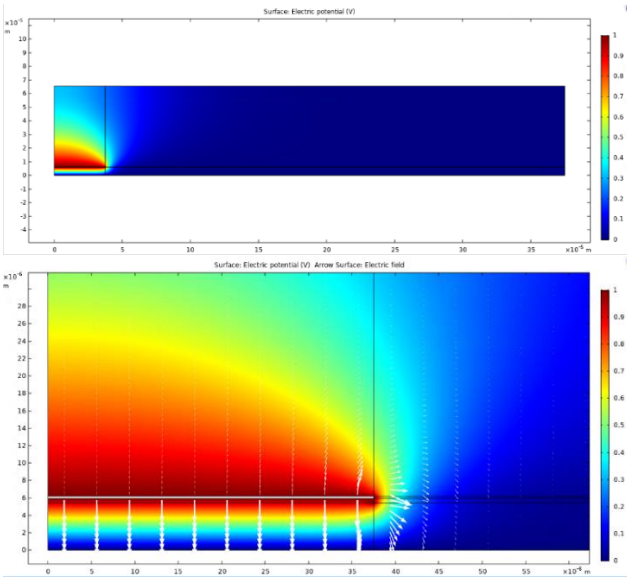
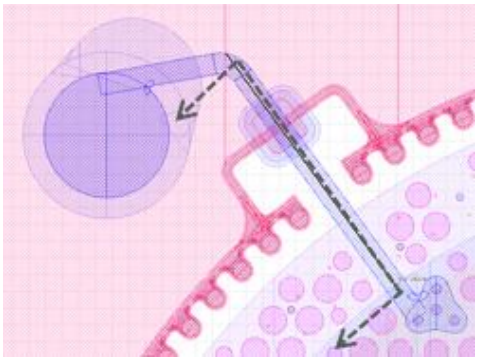


Fig.10. Electric potential and electric filed distribution, electric field lines are indicated with white arrow marks.

The parasitic capacitance obtained with integral over the bond pad surface is 0.0310pF. This is the total Cds component as represented in figure 5.

The Cbs component i.e. the parasitic capacitance formed between the substrate and back plate consists of two terms which includes Cbs-Metal trace and Cbs-Bond pad. The Cbs-Metal trace is the parasitic capacitance due to the metal trace and Cbs-Bond pad is the parasitic capacitance due to bond pad.

The cross section of the metal trace which is connected to the back plate highlighted below is shown in the figure 11.



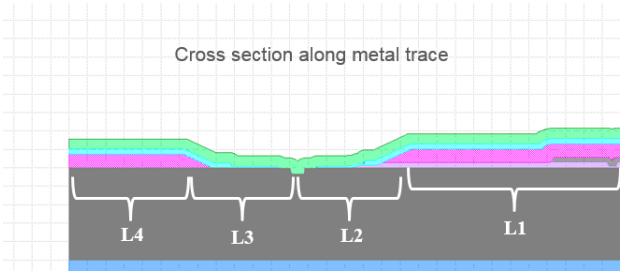


Fig. 11. Cross-section (highlighted portion) of the metal trace

A 3D model is set up in COMSOL Multiphysics® simulation software as shown in figure 12.

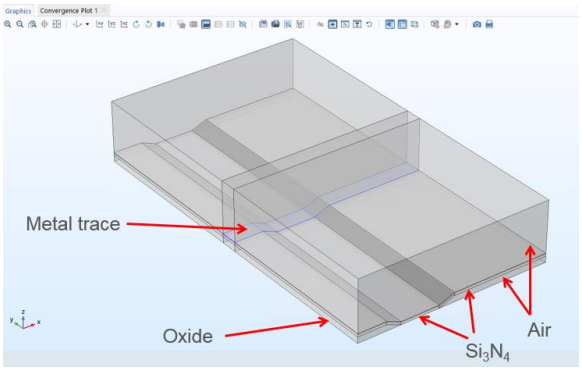


Fig.12. 3D model representation

Metal trace is represented as a ramp which replicates the actual trace in the cross section. End of trace is connected to bond pad which is not included in the model here. Since, the bond pad is of the same dimension here with respect to the previous bond pad parasitic capacitance estimation, it`s estimated parasitic is also approximated to be equal to 0.0310pF. The dimensions used in the 3D model for metal trace are tabulated in table 2.

Table 2

Parameters	Value
Si_3N_4 layer thickness	2.45 um
PSG/Oxide layer thickness	5.425 um
Metal thickness	0.25 um
Metal trace width	15 um
L1	160 um
L2	28 um
L3	28 um
L4	26 um

The model is evaluated in the Electrostatics physics set up with electric potential of metal trace set to 1V and substrate set to ground i.e. 0V.
The electric potential and electric field distribution (highlighted with white arrows) obtained with the stationary study is as shown in figure 13.

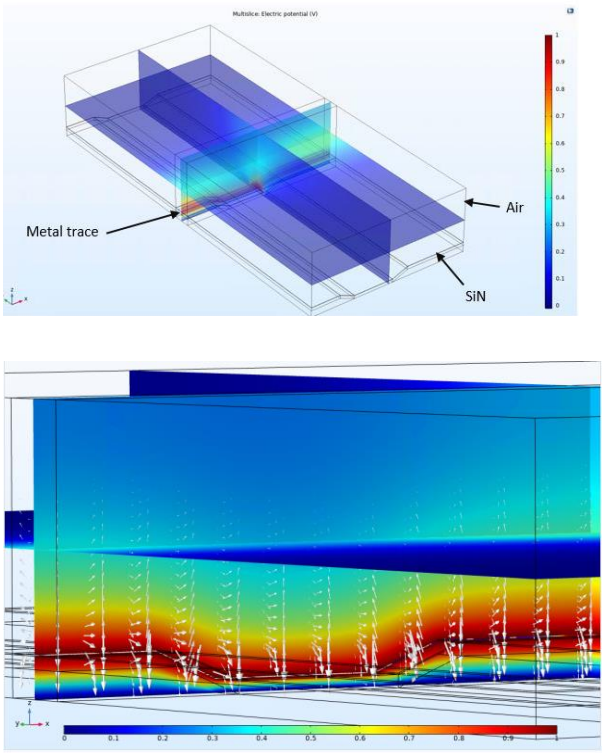


Fig 13. Electric potential and electric field distribution (zoomed) shown near the slope of the metal region

The parasitic capacitance obtained by taking integral of the surface over the metal is 0.0480pF.
The relative permittivity of the materials used in the models are tabulated in table 3.

Table 3

Material	Relative Permittivity
Air	1
Silicon Oxide	4.2
Polysilicon	4.5
Silicon nitride	9.7

Analytical Approach

The regions where metal trace sits can be categorized into 4 different sections as illustrated in figure 11: constant air gap (L1), sloped air gap (L2), sloped solid gap (L3), and constant solid gap (L4). Two simplifications are made here: First, the sloped regions are assumed to contribute 100% more unit capacitance than the flat regions. Second, the nitride layer is normalized with respect to air and PSG/oxide layer. The resulting wire capacitance is shown below:

$$Cwire = (L1 + 2 * L2)\left[\frac{w\epsilon o}{t.SiO2+\frac{t.SiN}{9.2}} + 2\pi * \frac{\epsilon o}{\log\left(\frac{t.SiO2+\frac{t.SiN}{9.2}}{Hmetal}\right)}\right] + (L4 + 2 * L3)\left[\frac{w.\epsilon SiO2}{t.SiO2+t.SiN\left(\frac{4.2}{9.2}\right)} + 2\pi * \frac{\epsilon.SiO2}{\log\left(\frac{t.SiO2+t.SiN\left(\frac{4.2}{9.2}\right)}{Hmetal}\right)}\right]$$

The fringing field effects on the capacitance of a circular parallel-plate capacitor cannot be ignored since the metal pad has a significant circumference. The contribution of capacitance due to the fringing field near the periphery of the pad can again be approximated

$$Cpad = \left[\epsilon.SiO2 * \frac{\pi r^2}{t.SiO2+t.SiN\left(\frac{4.2}{9.2}\right)}\right] + [\pi \epsilon.SiO2 * (2\pi r)\frac{1}{\log\left(\frac{t.SiO2+t.SiN*\left(\frac{4.2}{9.2}\right)}{Hmetal}\right)}]$$

where *r* denotes the radius of the pad. [3]

Results

The Finite Element Modeling results obtained using Comsol Multiphysics® software is tabulated in the table 4 below.

Table 4

Total C_{ds} = (C_{ds} Bond pad + C_{ds} Diaphragm_Substrate_Overlap)	0.0310pF+0pF= **0.0310pF**
Total C_{bs} = (C_{bs} Metal trace + C_{bs} Bond pad)	0.0480pF+ 0.0310pF= **0.079pF**
Total Parasitic Capacitance	0.0310pF+ 0.079pF= **0.11pF**

The analytical calculations based on the expressions defined, calculates the total capacitance to be 0.1094pF which is very close to the total parasitic capacitance calculated using FEM simulation. Table 5 compares the experimental measured result with analytical and simulation.

Table 5

	Experimental data (Median)	**Analytical Calculation**	**FEM Simulation**
Total Parasitic Capacitance	0.12pF	0.1094pF	0.11pF

The obtained results with the analytical calculation and FEM using Comsol Multiphysics® Software simulation is within ~10% of the measured value experimentally.

Conclusion

The simulation results align closely with the measured experimental data and analytical calculation. Thus, the simulation tool is useful when it comes to predicting the parasitic capacitance in MEMS microphones within permissible error. Needless to say, it can be extended to other capacitive sensing MEMS transducers as well. Future work can be done to improve accuracy of the model to match experimental data results.

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