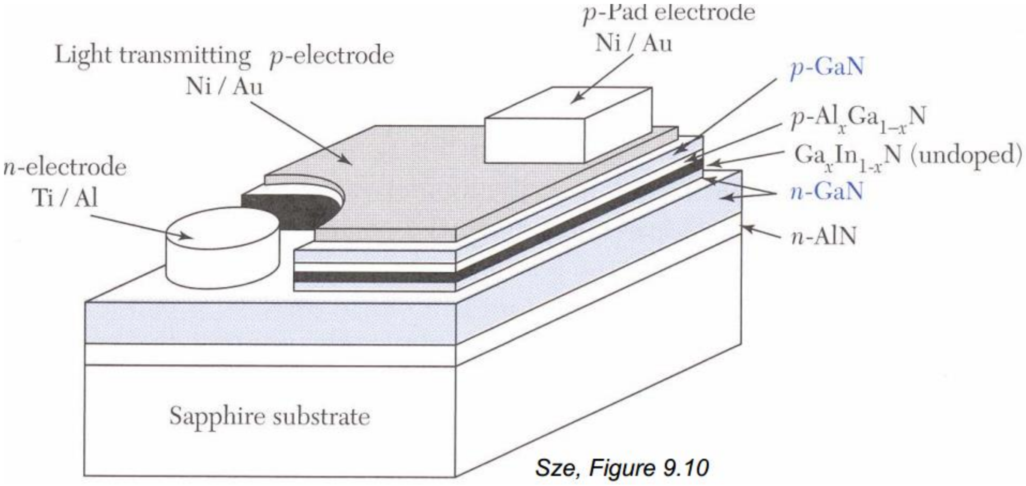
Thermal Model and Control of Metal-Organic Chemical Vapor Deposition Process

Jon L. Ebert, Sarbajit Ghosal, and Narasimha Acharya

SC Solutions, Inc.
1261 Oakmead Pkwy.,
Sunnyvale, CA 94085.

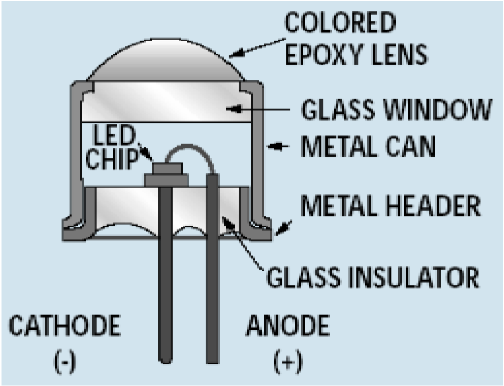
jle@acsolutions.com
https://www.scsolutions.com

Multi-Quantum Well Light Emitting Diodes (MQW-LED)



Sze, Figure 9.10

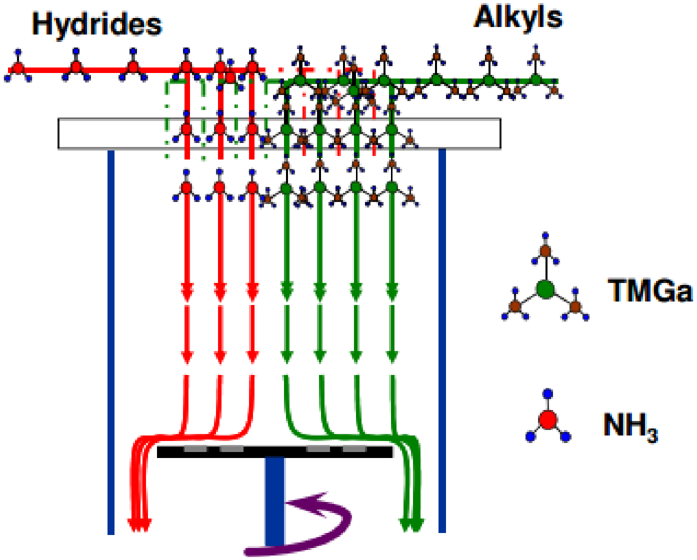
S.M. Sze and Kwok K. Ng, *LEDs and Lasers*, John Wiley & Sons, Inc., 2006.

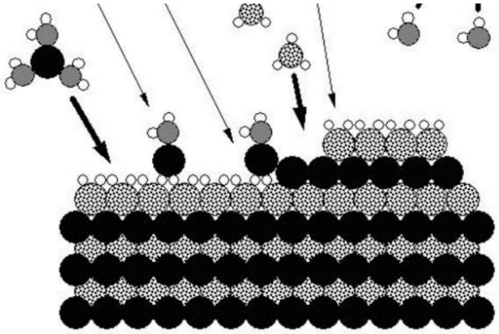


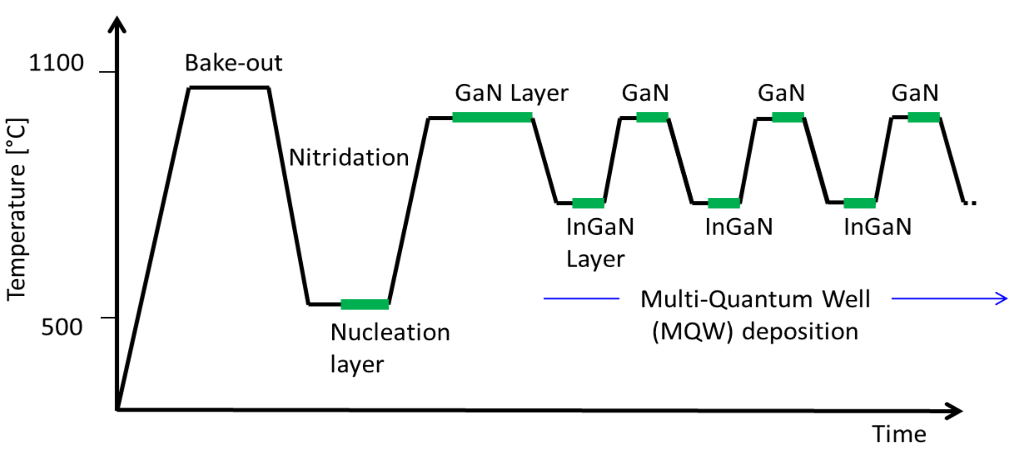
R. Stevenson, "The LED's Dark Secret," *IEEE Spectrum*, August 2009.

- **LEDs used in lighting are Multiple Quantum Well (MQW) devices that are fabricated on sapphire or silicon substrates.**
- **Several Indium Gallium Nitride (InGaN) quantum wells sandwiched between Gallium Nitride (GaN) quantum barrier layers.**
- **Frequency (color) of emitted light may be tuned from violet to amber by varying relative In/Ga fraction.**
- **After deposition, wafer diced into small rectangular chips (die), wire bonds (or other electrical leads) are inserted. Phosphor added as suspension or coating for white LEDs.**

Metal-Organic Chemical Vapor Deposition (MOCVD) of LEDs

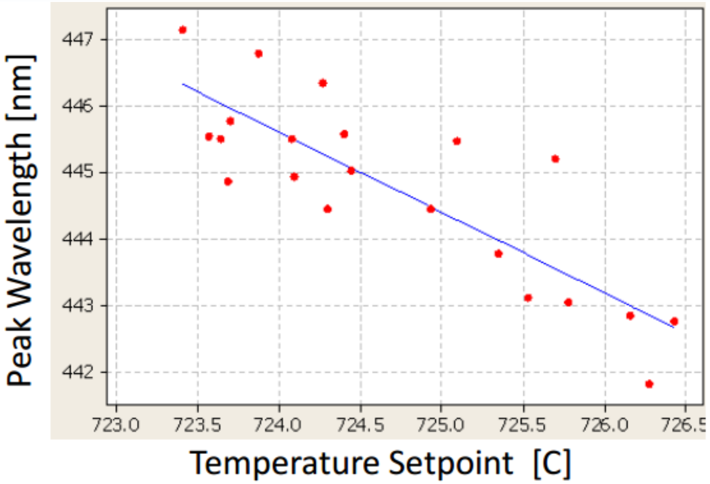




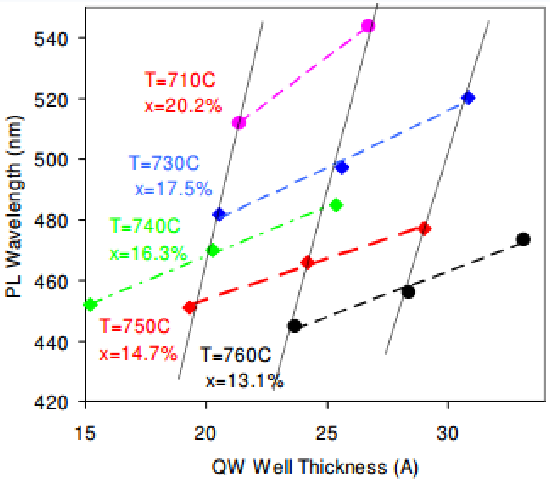


- ☐ Wafers (2”-6” diameter) rest in pockets in graphite susceptor (carrier) heated from below.
- ☐ Hydrogen carrier gas inflow through showerhead with dilute mixture of metal organic precursors, Tri-Methyl Gallium (TMG) and Tri-Methyl Indium (TMI) at 50-500 torr.
- ☐ Reactive gases decompose and deposit thin epitaxial layers (thicknesses range from a few nm to a few μm).

Cause of Color Variation in LEDs, LED ‘binning’



W. E. Quinn, *Driving Down HB-LED Costs*, Final Technical Report in fulfillment of the requirements of Department of Energy Grant DE-EE0003252, 2012.

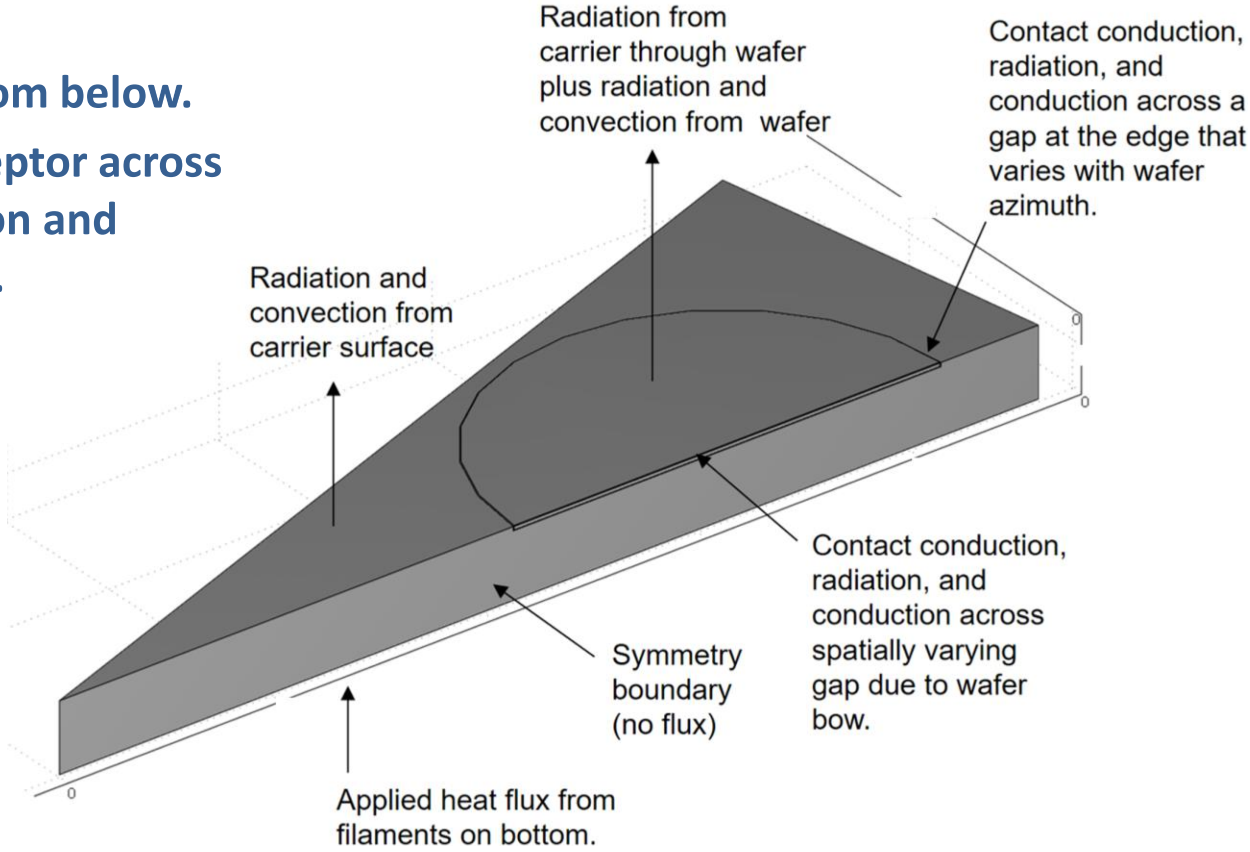


W. E. Quinn, “Trends in Production Scale MOCVD Systems to Reduce the Cost of Solid State Lighting,” Presentation at Semicon West, 2010.

- **Process variations have significant impact on color, lumens, and forward voltage of LEDs.**
- **Color of light emitted by LED is a strong function of the wafer temperature during deposition.**
- **Despite excellent control of susceptor temperature, light color varies significantly for chips fabricated on same wafer.**
- **To address this problem, LED manufacturers group devices into “bins”.**
- **Each bin spans a range of color temperature, voltage or lumens. Larger bin size means greater variation in light color or output – smaller bins have tighter control.**
- **For continued rapid increase of LED’s share of lighting market, it is necessary to significantly reduce, and preferably eliminate, the need for binning LEDs.**

What Causes Temperature Variation Across Wafer?

- ☐ Susceptor is heated from below.
- ☐ Wafer heated by susceptor across gap, cooled by radiation and convection on topside.

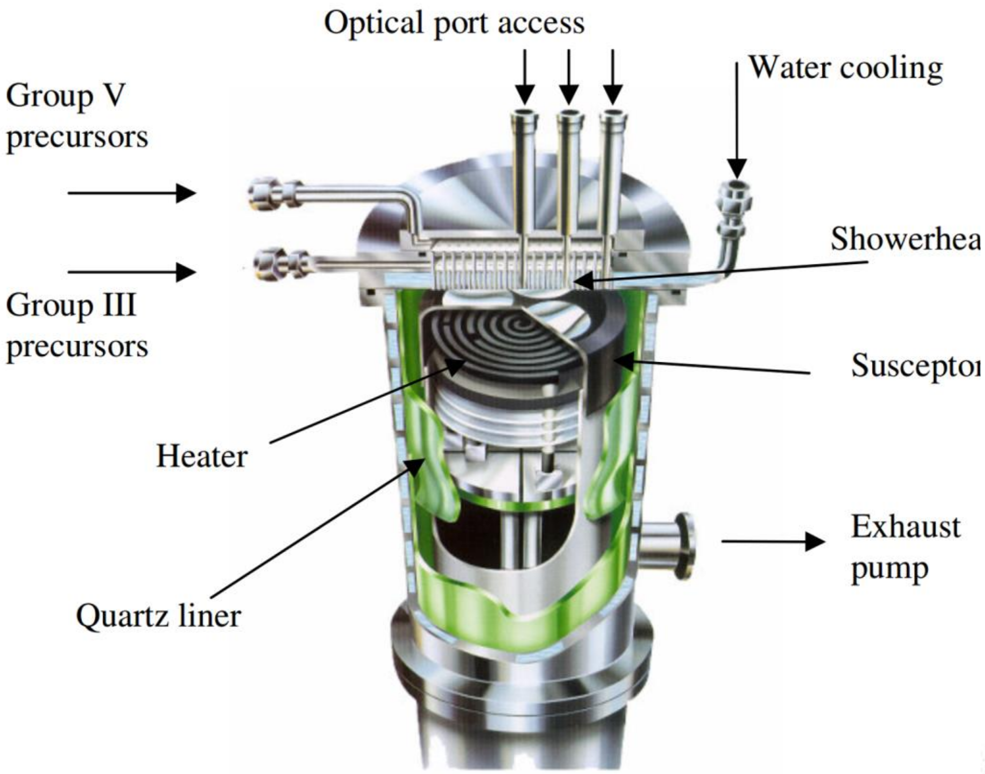


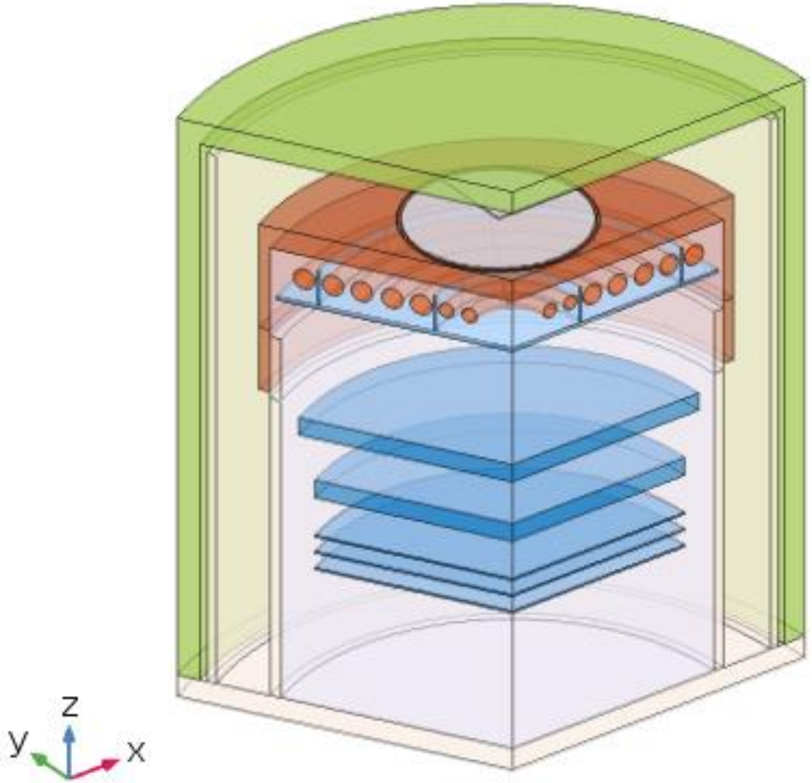
Using this COMSOL model, we show:

- ☐ Temperature gradient through wafer thickness causes wafer to bow (edge high).
- ☐ Wafer bow causes carrier/wafer gap to vary with radius from center of wafer.
- ☐ Variable gap size causes in-plane, radial temperature gradient.

Aixtron (Thomas Swan) 3 x 2” Reactor

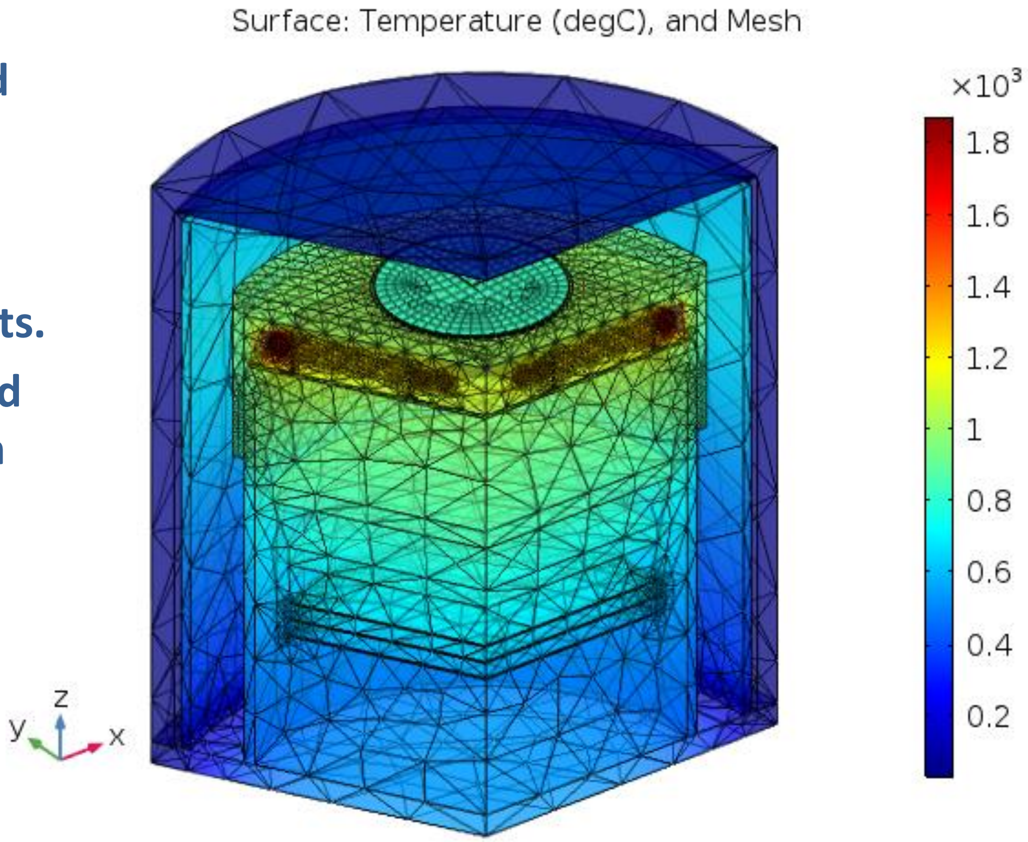
3D COMSOL model of one-third of the relevant part of the reactor was developed taking advantage of azimuthal symmetry.





COMSOL Model

- **Heat Transfer (with Surface-to-surface Radiation) and Solid Mechanics modules were used. Effect of flow modeled with correlation as explained in next slide.**
- **Mesh convergence tested for wafer temperature. Coarse mesh used in regions with low temperature gradients.**
- **Thermal contact between 2” wafer and susceptor modeled as H_2 layer with an additional thin layer bow of 26 μm depth.**
- **Operating conditions:**
  - 800°C nominal wafer temperature.
  - Pressure of 500 Torr.
  - Susceptor rotation rate of 500 RPM.
- **FEM model has 81.3K elements, and 135K DoF. Solution time is about an hour.**



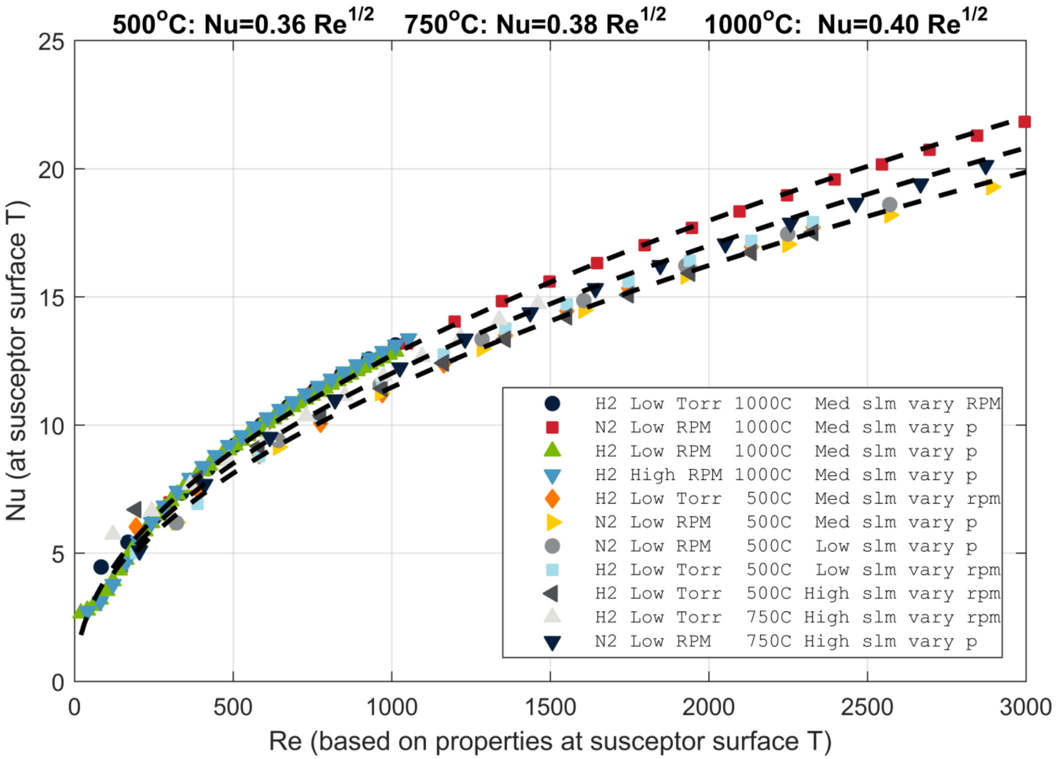
Surface: Temperature (degC), and Mesh

Correlation for Convective Cooling of Susceptor and Wafer

- **Gas flow not solved here because sufficient mesh refinement for flow increase surface number in surface-to-surface radiation which, in turn, greatly increases computation time.**
- **Instead, a separate 2D axisymmetric COMSOL model was used to develop heat transfer correlations for stagnation flow heat transfer from a rotating susceptor over a range of operating conditions as shown below.**
- **The resulting correlation for heat transfer coefficient as function of temperature was used in the COMSOL model.**

$$h = kA(T)\sqrt{\frac{\rho\omega}{\mu}}$$

A(T) = (0.29815 + *T**8E-5), where *T* is in K



Re = Reynolds Number

ρ = gas density

ω = rotation rate, rad/s

R = susceptor radius

μ = gas viscosity, Pa s

Nu = Nusselt Number

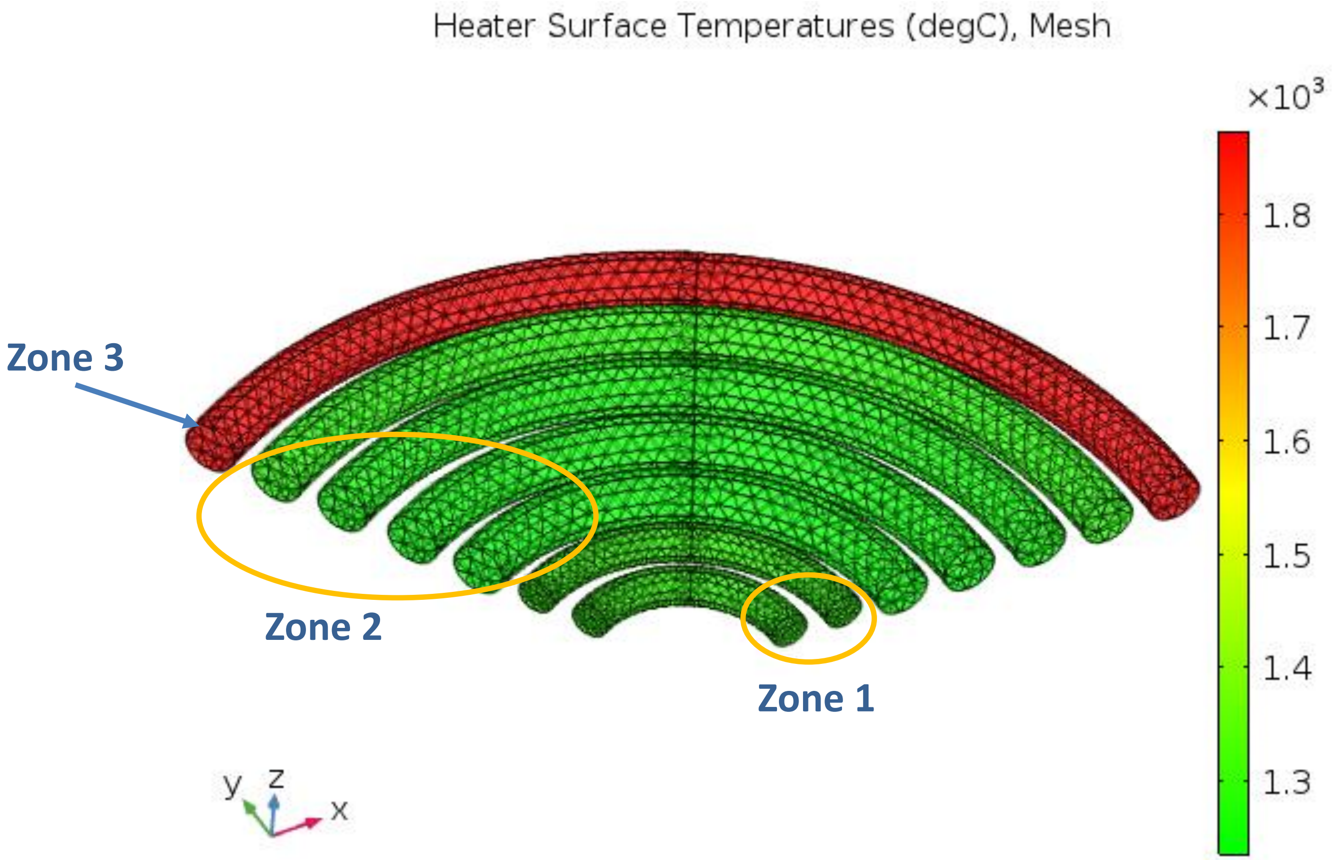
h = heat transfer coefficient, $W/m^2/K$

k = gas thermal conductivity

all properties evaluated at susceptor temperature

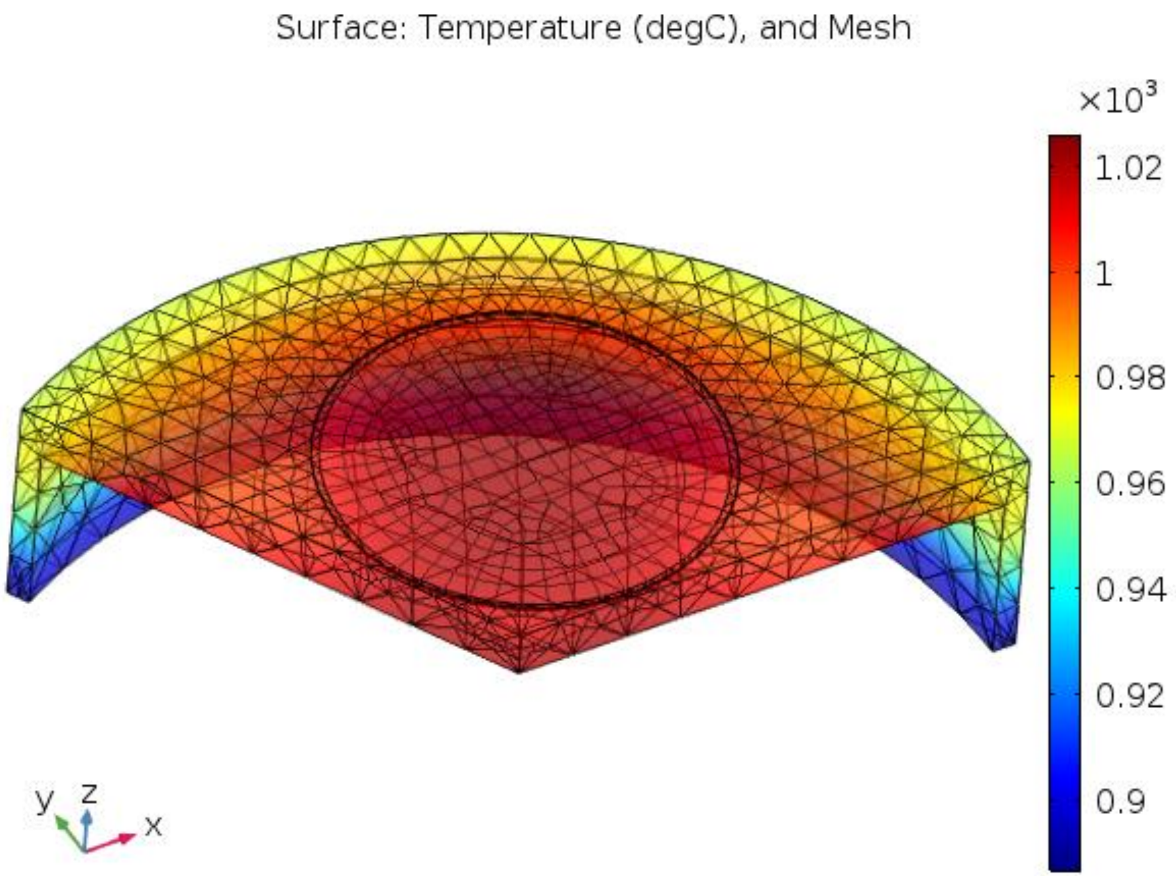
Heaters

- 7 heater coils grouped into 3 zones (Zone 1: innermost two coils, Zone 2: middle 4, and Zone 3: outermost coil).
- Each power zone coils vertically separated by ceramic plates.
- Baseline powers are : 48 W, 199 W, 823 W (divided among coils proportionate to coil volume).



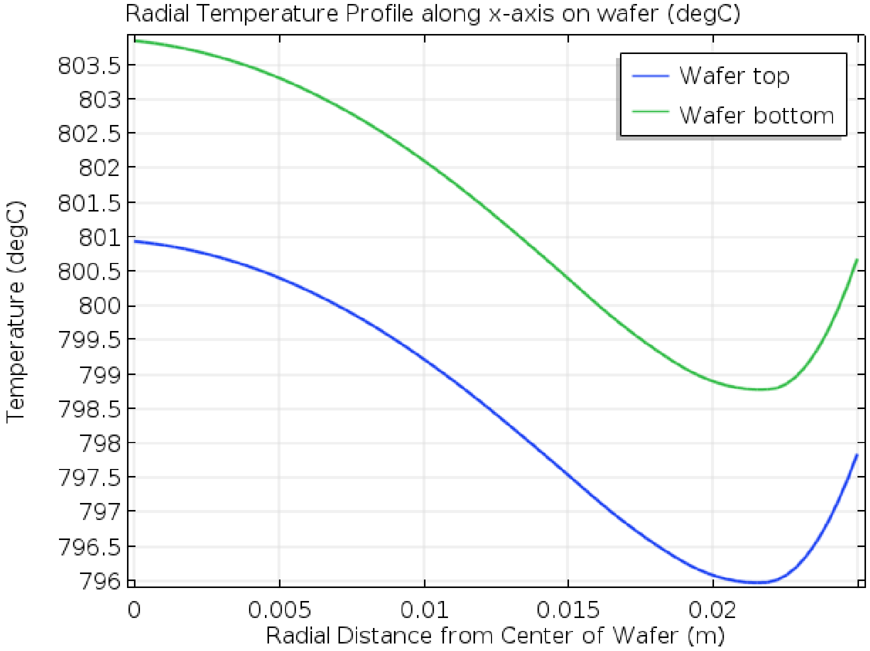
Susceptor Temperatures

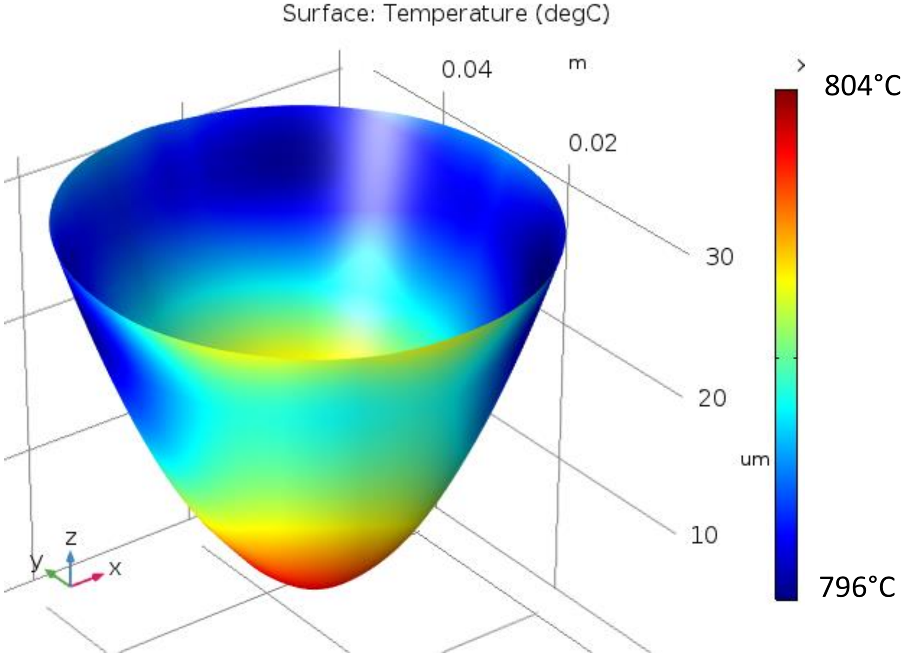
- ☐ Heated by radiation (and some conduction through nitrogen) from heaters.
- ☐ Loses heat radiatively to the surroundings walls and by convection to the process gases (modeled using heat transfer coefficient correlation).
- ☐ Maximum susceptor temperature is about 1025°C.



Wafer Bow

- ☐ Lower wafer surface is about 3˚C hotter than top.
- ☐ Resulting differential thermal expansion results in concave bow.
- ☐ This bow leads to the wafer top surface temperature non-uniformity.

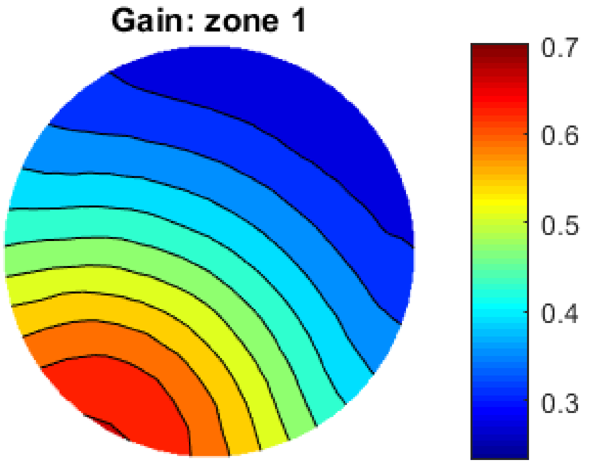


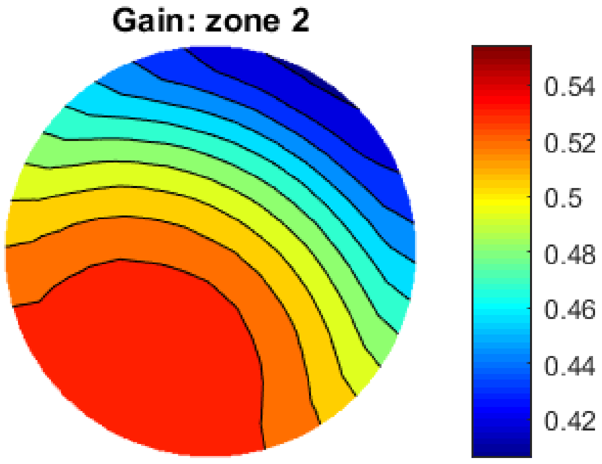


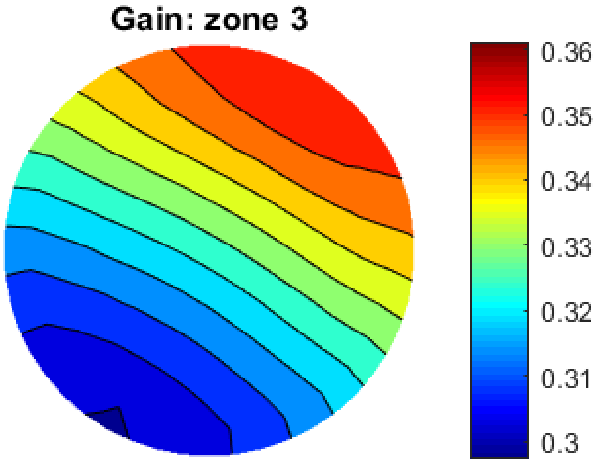
Vertical axis magnified for clarity.

Wafer Temperature Gains

Gains computed for each zone (units of °C/W).



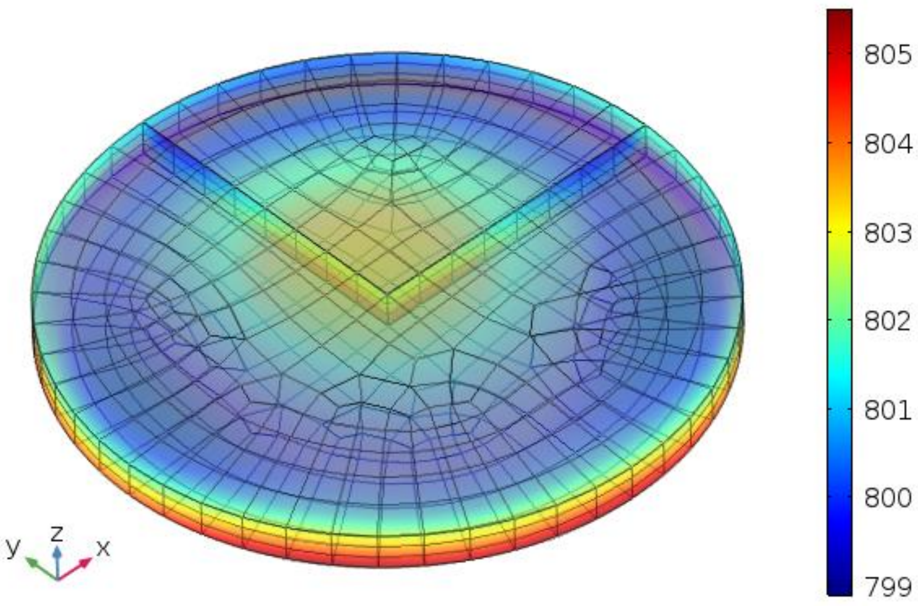




Best Wafer Temperature Uniformity

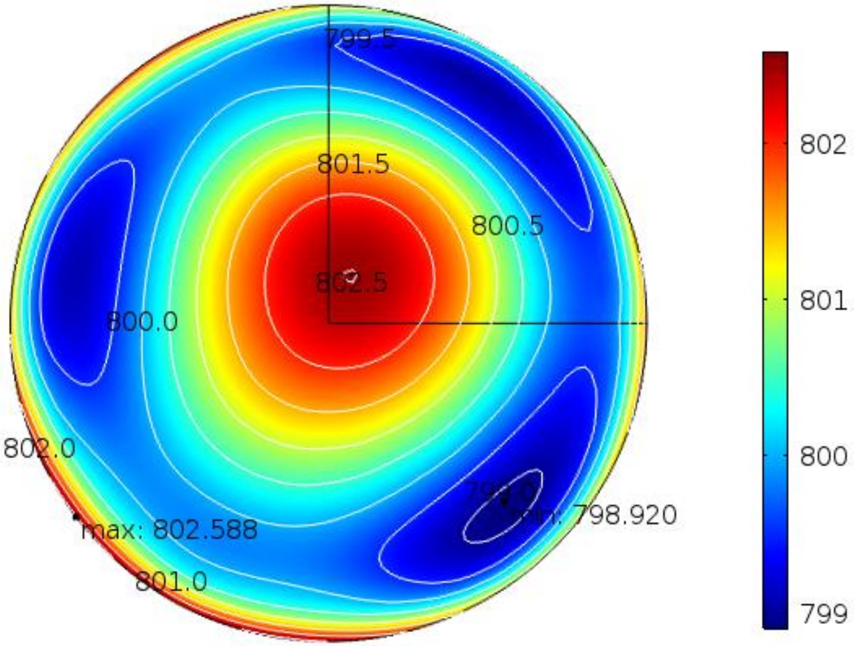
- **Temperature range with optimal power settings is less than 4°C on wafer top.**
- **Azimuthal asymmetry in wafer temperature non-uniformity cannot be corrected by heater power adjustments.**

Surface: Temperature (degC) Mesh



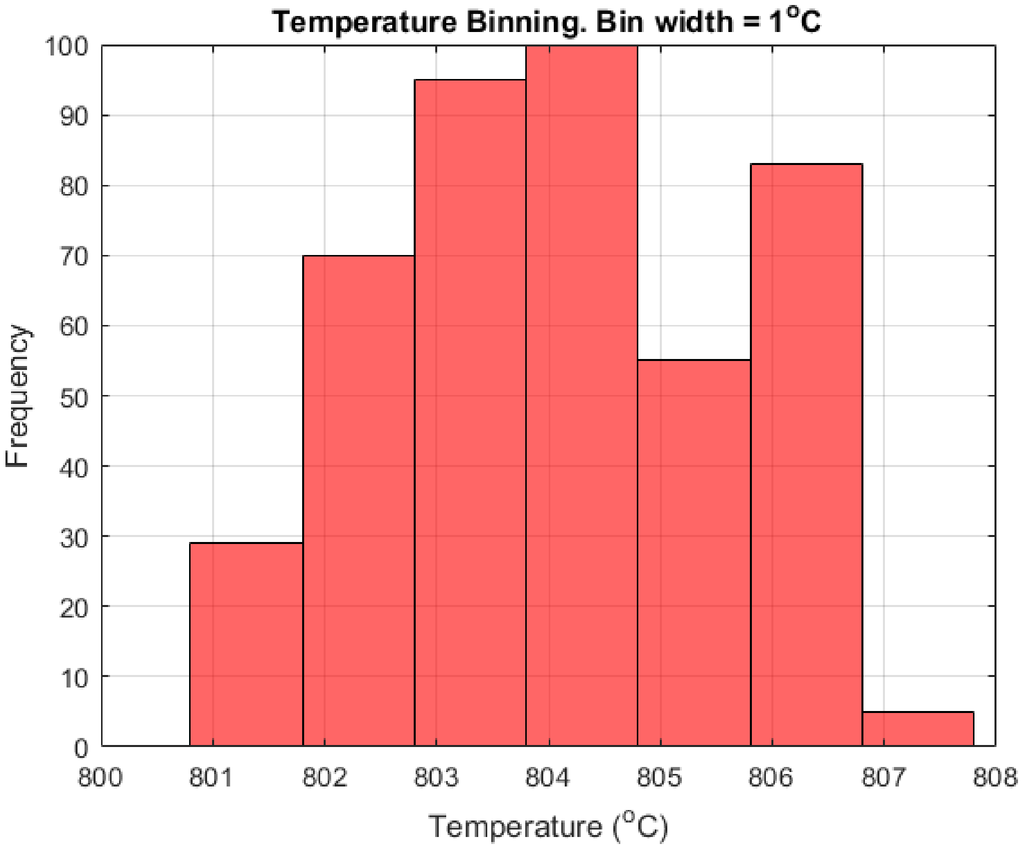
z dimension scaled up by factor of five.

Surface: Temperature (degC) Contour: Temperature (degC)
Max/Min Surface: Temperature (degC)



Temperature Binning

- ❑ Mesh in COMSOL model specifies temperatures at 618 points on top of wafer.
- ❑ These temperatures were binned into 7 bins that are 1°C in width.
- ❑ The challenge is to reduce the number of bins to one or two, i.e., within-wafer temperature non-uniformity to within 2°C or less.



Summary and Acknowledgement

- ☐ **COMSOL thermal model of MOCVD confirms that wafer bowing contributes substantially to within-wafer temperature nonuniformity.**
- ☐ **In the next step, we will validate model with experimental data.**

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