High Curvature Bending of Ultra-Thin Chips and Chip-on-Foil Assemblies

D. van den Ende[1]

[1]Holst Centre / TNO, Eindhoven, The Netherlands

Abstract

Introduction
Ultra-thin chips of less than 20µm become flexible, allowing integration of silicon IC technology with highly flexible electronics. This combination allows for highly intelligent products of unprecedented thinness, flexibility and cost. Examples include sensor systems integrated into food packaging or healthcare and sport monitoring tags as wearable patches or even directly in clothing textile [1]. During use the ultra-thin chips in these products can be bent to a very high curvature, sometimes to less than 1mm bending radius, which puts a large strain on the chips (see figure 1). In this paper the strength of ultra-thin chips at very high curvatures is evaluated, using a modified four-point bending method (see figure 2).

Use of COMSOL Multiphysics®
The Structural Mechanics Module in COMSOL Multiphysics® is used and modelling aspects of the four-point bending simulation are discussed including contact modelling with friction, initialisation settings -the chip is suspended freely in space at the start of the measurement - and solver settings. Results including the deformation and stress distribution in the chip are evaluated for different curvature levels during the test. Modelling the effects at high curvature are discussed, including contact and frictional effects at the chip-support interface at high deformation, so-called 'push through' effect.

The effect of chip thickness and geometry, bending direction and interconnections (see figure 3) on stress distribution in the chip is investigated using the developed method, for stand-alone thin chips as well as thin-chip on foil assemblies. The modelled stress distributions were compared to failures observed in experimentally tested thin chips. The model gives valuable insights into the reasons for the observed fracture mechanisms for thinned chips and chip-on-foil assemblies.

In conclusion the four point bending model was used as a calculation tool to verify chip strength under four point bending conditions and to obtain insights in chip failure mechanisms that occur during this bending test. For chip-on-foil assemblies it can be used to create design rules for creating more robust assemblies.

Reference

[1] D.A.van den Ende, A. Sridhar, et al, Integration techniques and applications of thin chips on low cost foil substrates, Proceedings of the 2013 Smart Systems Integration Conference, Amsterdam, March 2013

Figures used in the abstract

Figure 1: Ultra-thin chip bent between fingers (top left), Flexible monitoring tag (top right) and skin temperature sensor patch (bottom).

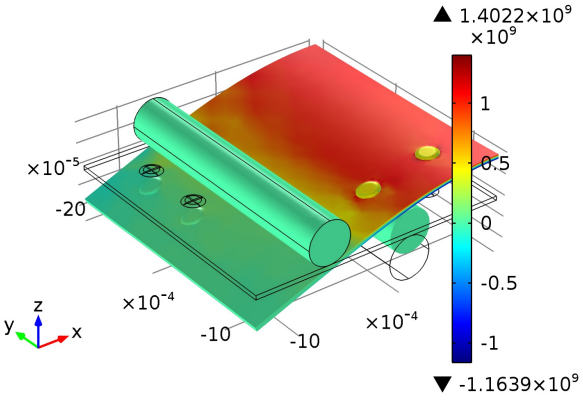

Figure 2: ¼ model of an ultra thin chip during 4 point bending loading showing the stress distribution (σ_x)

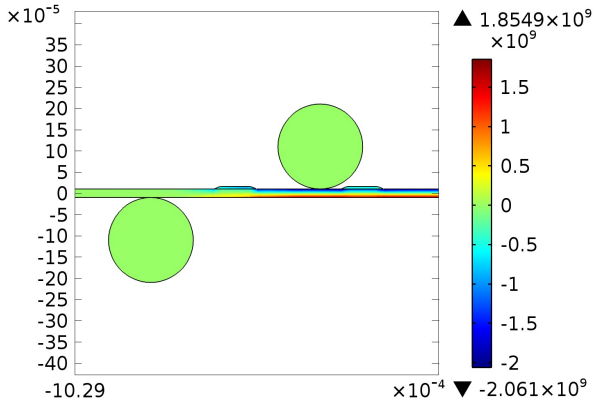

Figure 3: Cross section of an ultra thin chip during 4 point bending loading showing the influence of the interconnection bumps on the stress distribution